ABSTRACT OF THE DISCLOSURE

In a filter circuit of the present invention, a partial quantization value is computed by a quantization circuit according to a spread code and others in a unit at an arbitrary stage, where an integrating value is increased. The partial quantization value is successively added by an adder formed by a counter and is transmitted to a unit of the following stage. In an adder of the following stage, an analog residual is computed by subtracting an analog converted value of the partial quantization value, that is obtained by a D/A converter, from the integrating value so as to suppress an increase in the analog cumulative value. With this arrangement, in a matched filter in which spread spectrum receive signals serving as successive analog input signals are inputted on a time series and a correlation computing unit multiplies the time-series data by the spread code of a code sequence, the cumulative value is increased according to an increase in the number of taps, so that an analog adder can reduce power consumption, which is caused by expansion of a dynamic range at the following stage.